A Readout System Utilizing the APV25 ASIC for the Forward GEM Tracker in STAR

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Abstract—We have developed a modular readout system for the 30,720 channel Forward GEM Tracker recently installed in the STAR Experiment at RHIC, BNL. The modular architecture is based on a passive compact PCI backplane running a custom protocol, not PCI, connecting 6 readout modules to a readout controller module. The readout modules provide all necessary functions, including isolated power supplies, to operate up to 24 APV25 chips per module with high-impedance ground isolation. The front-end boards contain a minimal set of components as they are located inside the STAR TPC inner field cage and are inaccessible except during long shutdown periods. The front-end boards connect to the readout modules with cables up to 24 m in length, carrying unbuffered analog readout signals from the APV25 as well as power, trigger, clock and control. The readout module digitizes the APV analog samples to 12 bits at 37.532 MHz, and zero suppresses and buffers the data. The readout controller distributes trigger and clock from the central trigger system, gathers the data over the backplane, and ships it to a linux PC via a 2.125 Gbps optical data link (Detector Data Link (DDL) from ALICE). The PC gathers data from multiple readout controllers and dispatches it to the STAR event builders. The readout modules, controllers, and backplanes are housed in a common crate together with the GEM HV bias power supplies.

I. INTRODUCTION

The Forward GEM Tracker (FGT) for the STAR experiment at the Relativistic Heavy Ion Collider at BNL is a low-mass inner tracker for the forward region (partially) installed in the fall of 2011 as part of an overall STAR tracking upgrade plan. A driving goal of the FGT is to provide the tracking precision for charge discrimination between high momentum e(-) arising from W(-) boson lepton decay into an electron and a neutrino (or the corresponding anti-particles). W(-) are produced in high energy pp collisions via $\vec{A} + u$ ($\vec{b} + d$) interactions. When studied with longitudinally polarized proton beams, W(-) production parity violating asymmetries are an ideal tool to study the spin-flavor structure of the proton and hence an important part of the spin physics program at STAR. More generally, the FGT provides tracking for physics using the Endcap Electro-Magnetic Calorimeter (EEMC) that is located in the forward (pseudorapidity $1 < \eta < 2$) region of STAR.

The FGT, located inside the inner field cage of the STAR Time Projection Chamber (TPC), is a set of six independent triple-GEM detectors, with two dimensional readout, arranged in disks along the beam line on the side of the interaction region pointing toward the EEMC. Each disk is fabricated as four independent quadrants (see Fig. 1) pinned to a common support, and is designed in general to minimize dead material. For each quadrant, contained in its own working gas pressure volume with independent bias voltage divider board, a planar strip / pad (two dimensional readout) padplane fabricated on kapton film with two copper layers is used, in conjunction with the triple GEM structure, to detect the ionization signal of charged particle tracks and provide high spatial resolution (<100 µm) readout. The outer (inner) radius of the active area of an FGT quadrant is 381 (115) mm, while the perimeter frame is only 13 mm wide. The “Phi-projection” of charge is sensed with 720 strips on the padplane, while the “R-projection” of charge is sensed with 560 “lines” of pads interconnected with lines on the routing layer of the padplane, for a total of 1280 channels per quadrant. The front-end electronics assemblies, described in detail in section II,
effectively “straddle” the gap between quadrants, with four front-end assemblies per disk, and a common ground for the whole disk. This ground is locally isolated from the other disks and the support structures; each of the disks is grounded through its front-end cables to the substantial clean ground of the TPC front-end electronics nearby. The complete six disk FGT is 30,720 channels. The readout/DAQ system, described in detail in section III, consists of two major components: an APV Readout Controller (ARC) board and an APV Readout Module (ARM) board. These provide controls, trigger, clock, and power to the front-end electronics, digitize and process the signals, buffer the data and transmit to the STAR DAQ system. The ARC and ARM modules are linked by a custom protocol running on commodity CPCI backplanes, and are housed in a customized “VME” style crate together with the (commercial) GEM bias voltage supply modules.

II. FRONT-END ELECTRONICS

The APV25-S1 chip [1] is used for the FGT front-end readout. It consists of 128 channels of charge-sensitive preamplifiers with selectable polarity, pulse shapers, and 192 timebin circular buffer analog memories. Internal logic marks timebins for readout according to a programmable latency offset from the trigger input, and the sampled data of marked timebins are multiplexed for non-zero-suppressed 128 channel readout over a single differential current-mode output. In the FGT application of the APV25 we are typically reading 9 timebins at a latency of 86 timebins (2.29 µs). Note that this is not to be interpreted as the STAR trigger latency – it includes contributions from pipeline and cable delays in this readout system as well.

The analog sample data is accompanied by digital data (memory address and error status bit) and framing information encoded simply as binary data on the analog output. These binary high and low levels also serve as references to define the valid range of the analog signal. Since the timing from the clock to the binary data is the same as that to the analog data, it also serves as the standard signal for design of the readout board line receiver circuit, and for tuning of the ADC clock phase in the operational system.

The APV25 was developed by Rutherford Appleton Lab for the CMS silicon tracker, and has previously been applied to readout of a triple GEM tracker in the COMPASS experiment [2]. The design of the STAR FGT GEM foils, pad plane, and other elements of the detector generally follows the experience of COMPASS [3]. Within the STAR experiment we will also use the APV25 and essentially the same readout system described in this paper for the GEM Monitor Tracker (GMT) to be installed in 2012 and for the Inner Silicon Tracker (IST) to be installed in 2013.

To facilitate a low-cost front-end board and the ease of application of the APV25 to various projects, excepting the STAR IST which requires bare die, we have developed a BGA package (Fig. 3) for the chip in collaboration with an industry partner. The 15 mm × 20 mm package has 315 tin-lead 0.45 mm diameter solder balls on a 0.8 mm pitch. The package substrate is a 4 layer design with 50 µm trace width and spacing, using Nelco 4000-29 material. Of the 315 balls, 39 serve only for mechanical support. The 128 input balls are arranged 4 rows deep along a long edge of the package, with some wrap around. This layout permits routing out all of the input channels using only two signal layers on application front-end boards. An array of 81 balls directly connected to the die attach pad facilitates excellent thermal and electrical contact to the negative power plane in front-end boards.

The packages were assembled with known good die, wire bonding with 25 µm gold wire, and using a dam and fill encapsulation (Hysol FP4450/4451). A total of 575 packages were assembled to meet the needs of the FGT, GMT, and several other projects. A test board utilizing a custom BGA test socket was constructed and a basic functionality test done on all the assembled APV25 BGA’s; yield was 94%.

![Fig. 3. An APV die wire bonded on the BGA package substrate, before encapsulation. (Note the picture does not show the whole extent of the package substrate, it is 15 mm wide as seen here but 20 mm tall.)](image-url)

The FGT front-end board (Fig. 2) utilizes 5 APV25 BGA chips to read out 640 strips and pad-rows from one half of an FGT quadrant. The signals come in from a set of 1.0 mm pitch card-edge connectors mounted to the FGT pad plane, with the...
ground carried on copper strips from the detector ground plane (gas volume foil) to press-fit “PEM” nuts soldered to the front-end board at two locations. There are no active components on the front-end board apart from the APV25 chips and an I°C temperature sensor. The board is 260 mm x 40 mm, 1.6 mm thick FR-4 with four 17 µm copper layers (including two plane layers). The first assembly lot exhibited problems with open solder joints that were traced to warpage of the BGA packages due to moisture absorption; instituting a requirement to bake the packages immediately before assembly entirely resolved the issue.

At the outer radius of the FGT an ‘interconnect board’ straddles the gap between two quadrants, connecting to two front-end boards. Four interconnect boards with eight front-end boards serve each FGT disk (refer to Fig. 1). The interconnect board buffers the clock and trigger signals for the APV25 and connects to the cable going to the readout module. This board also contains a low-noise low-dropout linear voltage regulator to provide +/- 1.25 V power to the APV25’s from a +/- 1.75 V remotely regulated input from the readout module (see below), and an additional temperature sensor. The analog output signals of the APV chips pass through the interconnect board unbuffered; they have a split termination to ground on the ‘terminator board’ at the inner radius of the FGT. The terminator board also terminates the buffered clock and trigger lines from the interconnect board. The external clock and trigger inputs have a split termination to ground on the interconnect board.

To minimize photon conversions in the inner tracking region of STAR, the first 3 m of cable is a custom construction using copper-clad aluminum wire. Considering as a figure of merit the radiation length divided by the resistivity, standard copper-clad aluminum wire (10% copper by volume) is superior to pure copper by a factor 2.65. Aluminum wire has been used in other inner detector applications [4] but the STAR FGT is unique in utilizing commercially fabricated cable with conventional insulation and jacket materials (FEP and silicone). The signal wires were chosen to be a relatively heavy 28 AWG (solid) to conservatively address solderability concerns. The thickness of the copper layer on 28 AWG is 8 µm. Our experience of terminating these wires was very positive, and in hindsight 30 AWG likely would have performed equally well. The power wires in this cable are 22 AWG solid copper-clad aluminum. They are easily stripped and soldered, but tend to fracture upon any tight bend, much more readily than the 28 AWG wires. This necessitated significant care in termination. Once outside the inner support structure and TPC inner field cage, the cable transitions to conventional copper cables (various lengths up to 21 m are used) with the signals carried on low-loss 24 AWG foam polyethylene twisted pair. To minimize cable diameter and cost, only an overall foil shield is used – the signal pairs are not individually shielded. This results in a detectable level of crosstalk but it is well within the APV noise level.

III. BACK-END READOUT AND DATA ACQUISITION

Two interconnect boards, in other words two groups of 10 APV chips, are served by the APV Readout Module (ARM), shown in Fig. 4. In view of other applications in STAR, in particular the IST, the readout module is actually designed to handle 12 APV per group, with 2 readout channels per group unused in the FGT readout system. The different detectors will have unique designs for front-end modules and cable systems, but all use a common design from the readout module forward, including common firmware and software.

![Fig. 4. The APV readout module, 6U x 220 mm. Note the 24 analog input channels at the bottom, 6 quad ADC’s and 2 front-end FPGA’s in the middle, and 2 pairs of front-end power supplies top center. The front-end interfaces through J2 (bottom right), and front-end clock, trigger, and FC interfaces are just above J2.]()

The readout modules are housed in a crate mounted in a rack on the electronics platform adjacent to the STAR magnet, where the majority of detector electronics systems and power supplies are situated. A standard 6U form factor is used, however with the 220 mm option of IEEE 1101.1. The extra depth is more practical for a high density multichannel mixed-signal layout, especially for a readout module using rear cabling. Rear cabling enables quick replacement of modules, if necessary, during a brief controlled access; it is also neater and saves aisle space on the electronics platform, since low loss twisted pair cables with the required ratings are inherently bulky. A secondary benefit of the 220 mm boards is that a unified crate design for the readout system and the GEM bias high voltage modules (Wiener / ISEG) is feasible, saving rack space and simplifying the slow controls system.

A. Digitization and Processing in the Readout Module

Each APV output signal is independently received with a high common mode impedance differential line receiver circuit based on the Analog Devices AD8130, including an equalization filter to restore some of the high frequency cable losses and improve settling time. Slow settling of the signal
transitions would otherwise result effectively in crosstalk between the time-multiplexed APV channels. An optional digital filter may be used to further improve settling; this is not used in the FGT but if the cable attenuation must differ for other applications the digital filter will be necessary. The equalized signal is passed through a 3rd order anti-alias filter with differential output and programmable level shifting, and is then digitized with a 12 bit ADC with programmable gain (voltage reference). The ADC sample clock and the APV sample/readout clock are both derived from the RHIC bunch crossing clock. (Since the APV remains live and sampling during readout it uses a common clock for both functions.) A sampling frequency of 37.532 MHz is used, which is four times the RHIC bunch crossing clock. This was chosen to provide sufficient samples to determine the leading edge of a signal pulse (with a typical peaking time of order 50 to 100 ns) and to remain close to the APV’s designed sampling frequency of 40 MHz. The APV25 has a half-rate output mode which was intended for multiplexing two APV outputs locally at the front-end boards in CMS; we utilize this in order to reduce the bandwidth requirements on our long cable run. We select the APV IC base addresses (which are defined by pin strapping) to all be even, which as a “side effect” synchronizes the half-rate output from all the APV’s and thereby reduces the potential for crosstalk in the signal cables. The ADC always runs at the rate of the APV clock, and the leading samples of the APV binary header are stored at full rate, after which the readout is decimated by 2 and only the significant sample (the second) is stored for each of the remaining half-rate output datapoints from the APV for that event. A complete frame of 128 channels (for a single timebin) plus header from the APV chip takes 7.46 μs.

Four channels of programmable phase shift covering more than a full period of the 37.532 MHz clock are implemented using a sawtooth generator and reference comparator inside a phase-lock loop, with four additional programmable threshold comparators observing the same sawtooth. Nonlinearity and delay setting crosstalk for the phase shifter are measured to be less than 0.5 ns. The phase shifted outputs drive the APV and ADC clocks of the two front-end groups served by the readout module. The APV clock phase may be used to provide a fine tuning of the APV sampling with respect to the physics signals in the detector, with the coarse tuning programmed in the APV latency register.

The ADC clock phase is normally adjusted to sample the APV output signal at an optimal flat and settled moment – however by using a range of settings any repetitive waveform such as the APV binary header can be reconstructed on finer time scales. This was done on the installed system in STAR, with the result in Fig. 5 and Fig. 6. This demonstrates a large margin of 53 ns − 38 ns = 15 ns during which the data is settled flat within 1%. Ideally the ADC timing is set to center on that for normal operation. In reality there is a skew of typically 3.6 ns (fastest to slowest) between APV’s within a group, due to cable skew and trace length variations in the front-end and readout modules, so not all APV data can be exactly centered in this way, but there is still quite a sufficient margin for this adjustment.

Fig. 5. Interleaved sampling of APV binary header digitized by the readout module using 20 steps of ADC clock phase. There are 100 independent events used for each step. The amplitude corresponds to 8 mA peak to peak differential at the APV output. The trace shown here stops at the moment when decimation begins.

Fig. 6. Detail of binary high level from Fig. 5. The full scale swing is settled within 1% after 38 ns. The clock residual evident here, with amplitude around 0.4%, is due to crosstalk in the long signal cable. There is no averaging here, the vertical spread of points is indicative of the noise level.

We employ a multiple-timebin readout enabling the determination of the pulse amplitude and the pulse timing (for background rejection) more precisely with an offline fit. In STAR Run 12, commissioning the partial FGT, we are using 7 timebin readout without zero suppression. (The APV is set for 3 timebin mode and triggered 3 times, to read 9 timebins total, and the readout module stores only the first 7 of 9.) Zero suppression in the readout board FPGA will be implemented on a pulse-by-pulse basis, so that the entire waveform is taken for a channel if any timebin exceeds the threshold. Thresholds for zero suppression are to be computed online in the data acquisition PC during pedestal runs and then uploaded to the APV readout modules for normal running. The hardware zero suppression will be important to reduce data transfer times on the readout crate backplane.
B. Power and Slow Controls for the Front-end

The APV readout module also integrates all the other functions required to operate the front-end board. Four fully isolated 1.75 V, 2.5 A remote-regulated DC/DC converters provide power to the two front-end assemblies. These are push-pull converters designed with a slew rate limiting controller chip for low noise operation. A secondary-side error amplifier with remote sense connections drives the primary-side current-mode control through an opto-isolator. The controller’s current sense input is also amplified and digitized with a 12 bit, 3.5 MSPS ADC. The primary current sense waveform contains sufficient information about the secondary load current and (via the duty factor) about the secondary voltage. Firmware in the readout module FPGA will in the future calculate these and make them available to slow controls software.

The APV25 ASIC slow controls interface complies with the Philips I²C standard; there are 17 read/write registers and 1 read-only error flag register. Apart from a power-on reset circuit, all operation is controlled through these registers. We bus the I²C lines across all 10 APV chips and additionally 3 I²C temperature sensors, and connect this to the cables without buffering. (Small series resistors and clamp diodes to VDD are included on the front-end interconnect board.) An opto-isolated I²C line interface circuit is realized on the readout module board, with the I²C interface protocol handled in FPGA firmware.

The front-end electronics and FGT detector is ground referenced locally (to the clean ground of STAR TPC) and therefore we have carefully ensured that all front-end interface elements of the readout board have a high common-mode impedance to ground and a high common-mode rejection ratio. Typical ground voltage noise in STAR between the electronics platform and the TPC structure is of the order of 0.5 V and extends up to a few megahertz.

C. Readout Controller and Data Acquisition

The APV Readout Controller module (Fig. 7) interfaces to 6 readout modules through a passive 7-slot CPCI backplane. Two readout controllers with two backplanes are used for the full FGT. A simple protocol controlled by a state machine in the readout controller FPGA pulls data for each event from each of the readout modules in turn, starting at a defined delay after the trigger. As presently configured for commissioning the FGT in Run 12, with non-zero-suppressed 7 timebin readout, the data size is 111 kB, transferred in 864 µs on a 32 bit bus at 33 MHz clock frequency. This will be increased to 66 MHz with some improvements to clock distribution on a revision now in progress for the readout controller. The readout module can buffer 4 or more events onboard so the backplane data transfer generally does not contribute significantly to the deadtime.

The event data assembled by the readout controller is sent to the data acquisition front-end computer using the data link modules that have been developed for ALICE. The SIU and corresponding D-RORC are developed by CERN and are commercially available from Cerntech [5], [6]. This event driven fiberoptic link works at 2.125 Gbps to provide up to 200 MB/s throughput per link. The DAQ1000 upgrade for STAR standardized around this hardware, with up to 6 fiber links feeding a single front-end DAQ PC. The FGT uses 2 links in total. The readout controller module provides a 128 MB main data FIFO implemented in DDR2 SDRAM, which will be increased to 1 GB in DDR3 SDRAM in the revision. There is a guaranteed maximum of 4095 outstanding events in the STAR trigger/DAQ system, and so the use of these large (yet inexpensive) FIFO’s completely decouples the DAQ link / PC busy from the detector busy. The FGT detector busy is completely deterministic from the timing of triggers which have been received. Operating experience from the FGT indicates a continuing need to support non-zero-suppressed readout with 7 timebins to complete the commissioning of the detector, and to do this without reducing the allowed number of outstanding events requires the larger FIFO.

Configuration and slow controls for the readout system, including APV configuration, temperature monitoring, etc., is handled through the DDL link between the DAQ PC and the readout controller. No dedicated slow controls hardware is necessary.

The readout controller module also incorporates the STAR trigger interface (receiving a 20 bit code and the RHIC collision clock over a 7-pair differential PECL cable), and four general purpose NIM inputs and four outputs, which have been of great value in setting up standalone test systems, e.g., for cosmic ray tests of the FGT. Lastly, there is an ethernet interface which is used to apply firmware updates and to access various diagnostic registers.

Fig. 7. The APV Readout Controller (ARC). The mezzanine card here is the DDL optical data link connecting to the data acquisition PC.
IV. CONCLUSIONS

The STAR forward GEM tracker readout system has been successfully installed and commissioned this year together with just over half of the forward GEM tracker quadrants. It is an innovative modular design applying the APV25 ASIC in the context of the STAR experiment at RHIC. We look forward to completion of the FGT and GMT during the 2012 summer shutdown, and the IST the following summer using this readout system. We also plan to leverage some of the details described herein to serve in future systems based on other front-end chips.

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