Belle-II

Internal Prototype Board Review

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November 22, 2011

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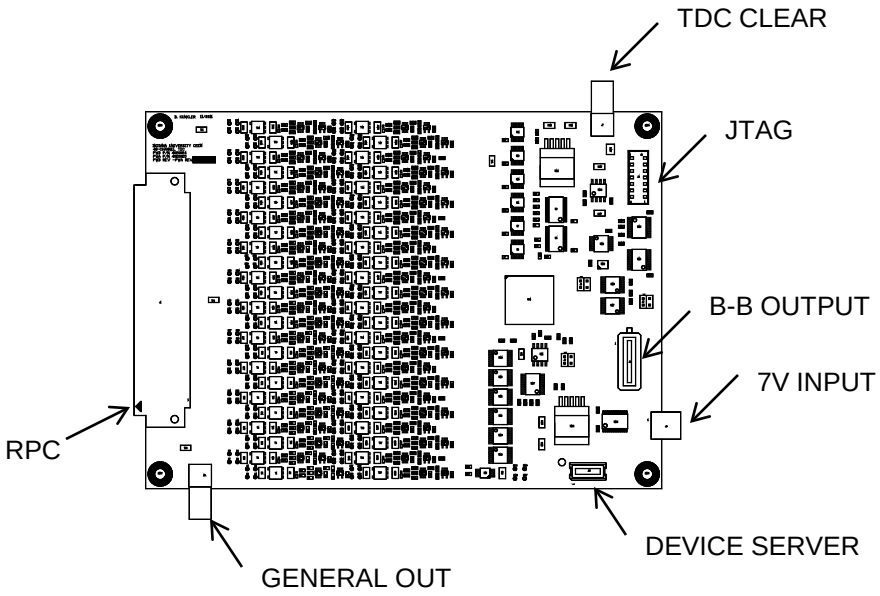
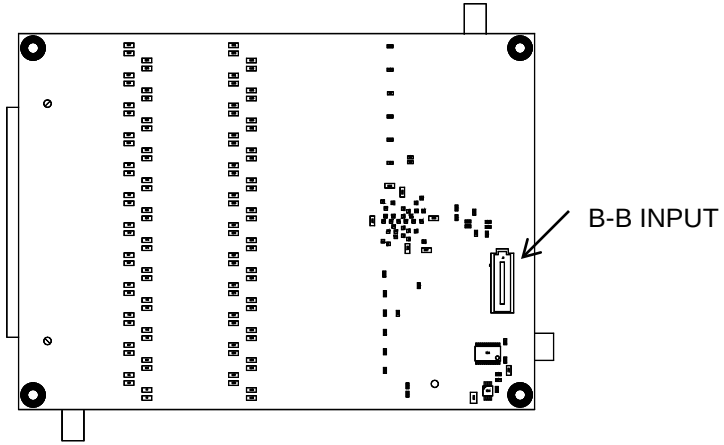
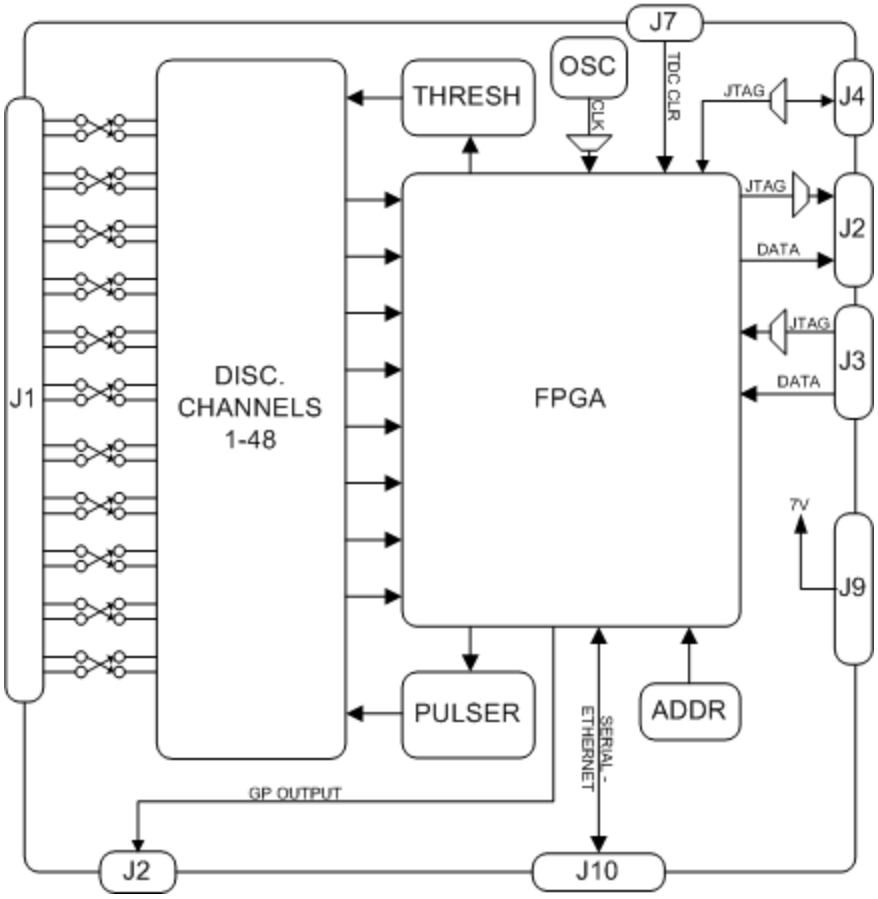
Prototype Assembly





- TDC Clear and General Out are Lemo connectors.
- The board-to-board-connectors (B-B) allow the boards to be stacked.
- The device server connector allows an Ethernet module to be installed.

Prototype Functional Diagram

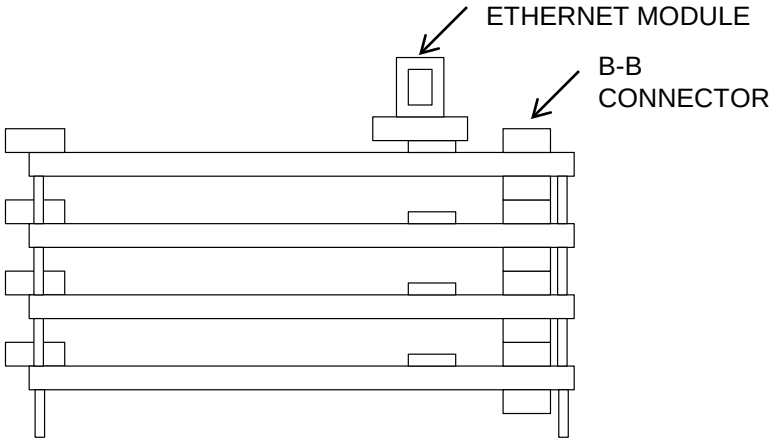


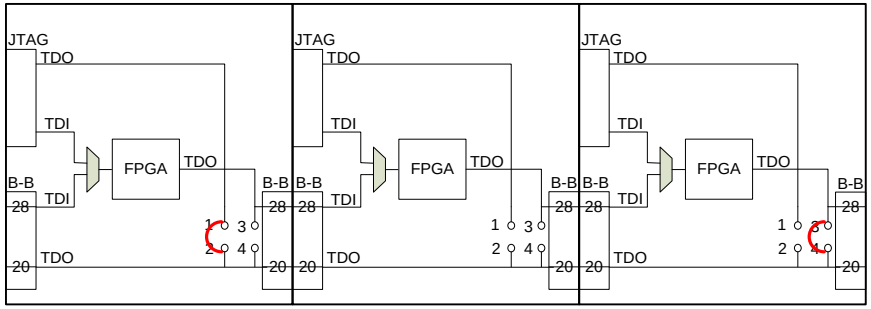
- RPC output polarity can be swapped.
- One B-B connector is input (J3), the other is output (J2) allowing data to be moved between boards.
- The B-B connectors are high-speed so the signal integrity will be similar to final 96-channel board.
- JTAG, clock, and data are multiplexed so there is one master in the stack.
- At least one board in stack may contain a Etherne module (serial-Ethernet device server).
- The threshold (THRESH) is controlled by six 8-channel DACs.

Nano LANReach 3-24Mbps Ethernet module with server.

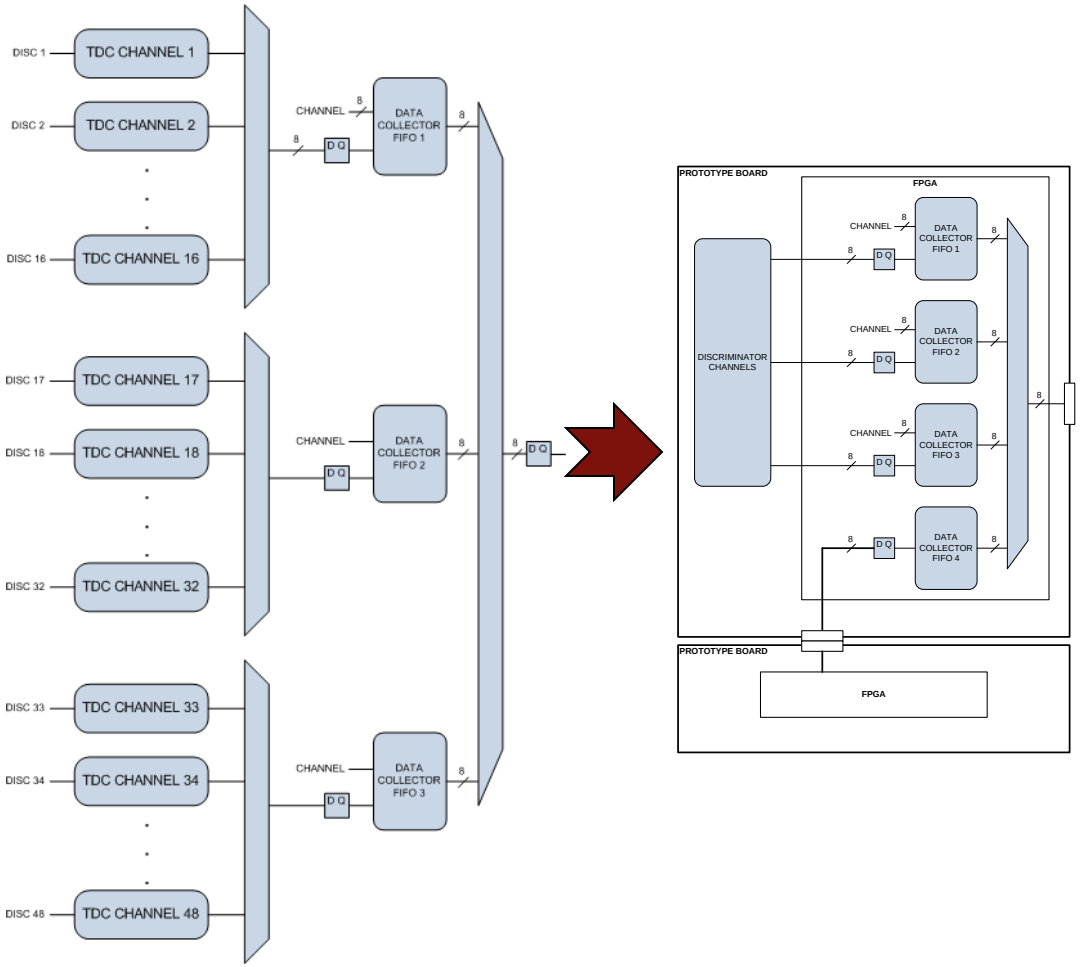
Stack-Up

- The top B-B connector is output and the bottom is the input.
  - Allows communications between boards
- The idea is we can stream data from the last board in the chain (bottom) to the first (top).
- Top board can contain an Ethernet module for streaming data to a PC.
  - Only requires crossover cable.
  - TeraTerm or Wireshark can be used to collect data.
- Top and bottom boards are special.
  - Jumpers allow use of ChipScope to collect data.





Top Level TDC FPGA



- Adding a fourth FIFO easily allows data to be streamed to next board.
- The TDC Channel contains a 16 deep FIFO with 8-bit input and 8-bit output.
- The Collector FIFOs are 256 deep with a 16-bit input and 8-bit output.

Performance

- Existing design – no board stack
  - 4 ns time resolution
  - 18 +/- 2 ns double pulse resolution
  - 528 ns maximum single channel latency due processing and pipelining
  - Simultaneous hit on each channel processed with 948 ns latency
  - Simultaneous hit on 4 channels processed with 347 ns latency
  - Data output is 8-bit channel value followed by 8-bit time value
- Board stack
  - Single channel latency increases to (528+4)*4 = 2128 ns if Ethernet module is used.
  - Simultaneous hit latency will increase accordingly.
  - Data output is 4-bit board address then 8-bit channel values followed by 8-bit time values.